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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/550,645

08/23/2006

Tominaga Koji

FUJ-0002

1944

23413 7590 09/23/2008  
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EXAMINER

MALEK, MALIHEH

ART UNIT

PAPER NUMBER

2813

NOTIFICATION DATE

DELIVERY MODE

09/23/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/550,645	<b>Applicant(s)</b> KOJI ET AL.	
	<b>Examiner</b> MALIHEH MALEK	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 29 April 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>04/29/2008</u> .  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

This office action is in response to the communication filed on 04/29/2008.

#### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-3 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In claim 1, the recitation; “... *the interface layer comprises an oxide of silicon formed so as to be mutually diffused with the silicon substrate, and a high dielectric constant metal element*” is not clear. Claim 1 is ambiguous in describing the mutual diffusion of the adjacent layers. Claims 2-3 and 6 are included likewise because they depend on claim 1.
- In claim 1, the term “*a high dielectric constant metal element*” is not clearly introduced if it is the same as the “diffusion suppressing layer” or it is a different layer.
- Claims 3 and 6 are indistinct; it is not clear that how the high dielectric constant metal constitutional element relates to the high dielectric constant insulating film.

Art Unit: 2813

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (***See MPEP Ch. 2141***)

- a. Determining the scope and contents of the prior art;
- b. Ascertaining the differences between the prior art and the claims in issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada (Pub. No.: US 2002/0195643 A1).

Regarding claim 1, Harada teaches a semiconductor device ([0001]) characterized in that an interface layer 11b (silicon oxynitride film containing hafnium), a diffusion suppressing layer 11a ( $\text{Hf}_x\text{Si}_y\text{O}_2$ ) and a high dielectric constant insulating film 11c (silicon-containing hafnium oxide film containing nitrogen) are sequentially formed in this order on one surface of a silicon

Art Unit: 2813

substrate 10; and the interface layer 11b comprises an oxide of silicon (silicon oxynitride film containing hafnium which prevents a reaction between the silicon substrate 10 and layer 11a) formed so as to be mutually diffused with the silicon substrate, and a high dielectric constant metal element ([0075]).

Regarding claim 1, Harada discloses the claimed invention except for that specifically teaches that the layer 11a is a diffusion suppressing layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have layer 11a as a diffusion suppressing layer since it is known in the art that high-k dielectric materials are suitable barrier layers which prevent the reaction between two adjacent layers.

Regarding claim 3, Harada teaches a semiconductor device wherein a high dielectric constant metal constitutional element in the constitutional element of the high dielectric constant insulating film is made the same as a part of the high dielectric constant constitutional element in the interface layer to prevent a reaction between the adjacent layers ([0075]).

Regarding claim 4, Harada teaches a method for manufacturing a semiconductor device ([0001]) comprising: forming, on one surface of a silicon substrate 10, an initial layer 11b which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion suppressing layer 11a ( $\text{Hf}_x\text{Si}_y\text{O}_2$ ) on the surface of the initial layer 11b ([0075]); performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon

Art Unit: 2813

substrate 10, thereby forming an interface layer (silicon oxynitride film containing hafnium which prevents a reaction between the silicon substrate 10 and layer 11a); and forming a high dielectric constant insulating film on the surface of the diffusion suppressing layer ([0022]); wherein the interface layer comprises an oxide of silicon. The device structure of Harada is the same as the device claimed. It can be assumed that the device will inherently be produced by the claimed process. See, for example, *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Regarding claim 5, Harada teaches a method for manufacturing a semiconductor device ([0001]) comprising: forming, on one surface of a silicon substrate, an initial layer which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion suppressing layer on the surface of the initial layer; forming a high dielectric constant insulating film on the surface of the diffusion suppressing layer ([0075]); and performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate, thereby forming an interface layer ([0022]); wherein the interface layer comprises an oxide of silicon. The device structure of Harada is the same as the device claimed. It can be assumed that the device will inherently be produced by the claimed process. See, for example, *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Regarding claim 5, performing heat treatment after or before forming the high dielectric constant insulating film is an obvious alternative since selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results; *In re Burhans*, 154 F.2d 690 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F2d 975, 5 USPQ 230 (CCPA 1930). MPEP 2144.04.

5. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada (Pub. No.: US 2002/0195643 A1) in view of Bai (Pub. No.: US 2001/0013629 A1).

Regarding claim 2, the previous combination remains as applied to claim 1 above.

However, regarding claim 2, the previous combination does not teach a semiconductor device wherein the interface layer has an equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or smaller.

In the same field of endeavor, regarding claim 2, Bai teaches a semiconductor device wherein the interface layer has an equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or smaller ([0020] and table I) to increase the capacitance of a gate dielectric without decreasing the performance of the device ([0012]). Bai discloses the claimed invention except for the exact value of the SiO<sub>2</sub> thickness of 1.0 nm or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an interface layer having equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or less, since it has

Art Unit: 2813

been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 6, Harada teaches a semiconductor device wherein a high dielectric constant metal constitutional element in the constitutional element of the high dielectric constant insulating film is made the same as a part of the high dielectric constant constitutional element in of the interface layer to prevent a reaction between the adjacent layers ([0075]).

### ***Response to Arguments***

6. Applicant's arguments filed on 04/29/2008 have been fully considered but they are not persuasive.

The applicant argues that Harada does not teach or suggest the interface layer comprising an oxide of silicon as claimed in claims 1, 4 and 5.

In response to applicant's argument, Harada teaches that the interface layer 11b, which prevents a reaction between the silicon substrate 10 and the high dielectric constant film 11a, may be made of for example a silicon oxynitride film containing hafnium. In claim 1, applicant claims "...the interface layer comprises an oxide of silicon...", knowing that silicon oxynitride film is an oxide of silicon, the applicant's argument is not persuasive. Furthermore, Harada introduces the silicon oxynitride as an



example for the interlayer 11b in paragraph [0075]; applicant is also referred to paragraph [0099] of Harada. While applicant argues that the interface layer 11b of Harada does not comprise an oxide of silicon, note that applicant is reminded that terminology in a pending claim is to be construed as broadly as reasonably possible, *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989), and the limitation from the specification will not be read into the claims, *Sjolund v. Musland*, 847 F.2d 1573, 1581, 6 USPQ2d 2020, 2027 (Fed. Cir. 1988).

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Art Unit: 2813

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MALIHEH MALEK whose telephone number is (571)270-1874. The examiner can normally be reached on Mon-Fri, 8:30-6pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on (571)272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/  
Supervisory Patent Examiner, Art  
Unit 2822

Sep. 16, 2008

/M. M./

Examiner, Art Unit 2813